

EL 366000049

EL 465782038

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

\* \* \* \* \*

Semiconductor Processing Methods Of Forming  
Transistors, Semiconductor Processing Methods Of  
Forming Dynamic Random Access Memory Circuitry,  
And Related Integrated Circuitry

\* \* \* \* \*

INVENTOR

Luan C. Tran

ATTORNEY'S DOCKET NO. MI22-878

1           **SEMICONDUCTOR PROCESSING METHODS OF FORMING**  
2           **TRANSISTORS, SEMICONDUCTOR PROCESSING METHODS OF**  
3           **FORMING DYNAMIC RANDOM ACCESS MEMORY CIRCUITRY,**  
4           **AND RELATED INTEGRATED CIRCUITRY**

5           **TECHNICAL FIELD**

6           This invention relates to semiconductor processing methods of  
7           forming transistors, to semiconductor processing methods of forming  
8           dynamic random access memory circuitry, and to related integrated  
9           circuitry.

10          **BACKGROUND OF THE INVENTION**

11          Semiconductor processing typically involves a number of complicated  
12          steps which include patterning, etching, and doping or implanting steps,  
13          to name just a few, which are necessary to form desired integrated  
14          circuitry. One emphasis on improving the methods through which  
15          integrated circuitry is formed, and which is directed to reducing the  
16          processing complexity, relates to reducing the number of processing steps.  
17          By reducing the number of processing steps, risks associated with  
18          processing mistakes entering into the processing flow are reduced.  
19          Additionally, wherever possible, it is also highly desirable to reduce  
20          processing complexities while providing added flexibility in the processing  
21          itself.

22          For example, several processing steps are required to form  
23          transistor constructions. One or more of these steps can include a

1 threshold voltage definition step in which one or more channel  
2 implantation steps are conducted to define the threshold voltage for the  
3 ultimately formed transistor. In some applications, it is desirable to  
4 have transistors with different threshold voltages. Typically, different  
5 threshold voltages are provided by additional masking and doping or  
6 implanting steps to adjust the doping concentration within the channel  
7 region of the various transistors desired to have the different threshold  
8 voltage. Specifically, one transistor might be masked while another  
9 receives a threshold implant; and then other of the transistors might be  
10 masked while the first-masked transistor receives a threshold implant.

11 This invention grew out of concerns associated with reducing the  
12 processing complexities involved in forming transistors having different  
13 threshold voltages.

## 14 15 SUMMARY OF THE INVENTION

16 Semiconductor processing methods of forming transistors, -  
17 semiconductor processing methods of forming dynamic random access  
18 memory circuitry, and related integrated circuitry are described. In one  
19 embodiment, active areas are formed over a substrate, with one of the  
20 active areas having a width of less than one micron. A gate line is  
21 formed over the active areas to provide transistors having different  
22 threshold voltages. Preferably, the transistors are provided with different  
23 threshold voltages without using a separate channel implant for the

1 transistors. The transistor with the lower of the threshold voltages  
2 corresponds to the active area having the width less than one micron.

3 In another embodiment, a plurality of shallow trench isolation  
4 (STI) regions are formed within a substrate and define a plurality of  
5 active areas having widths at least some of which are no greater than  
6 about one micron, with at least two of the widths preferably being  
7 different. A gate line is formed over the respective active areas to  
8 provide individual transistors, with the transistors corresponding to the  
9 active areas having the different widths having different threshold  
10 voltages. In an STI process, devices having width smaller than 1 micron  
11 typically also have a lower threshold voltage. This is referred to as  
12 "reversed narrow width<sup>1/</sup> effect as contrasted with the case of transistors  
13 formed using LOCOS isolation, where threshold voltage tends to increase  
14 as device width decreases.

15 In another embodiment, two field effect transistors are fabricated  
16 having different threshold voltages without using a separate channel  
17 implant for one of the transistors versus the other.

18 In yet another embodiment, two series of field effect transistors  
19 are formed, with one series being isolated from adjacent devices by  
20 shallow trench isolation, the other series having active area widths  
21 greater than one micron. The one series is formed to have active area  
22 widths less than one micron to achieve lower threshold voltages than the  
23 other of the series.

1 In yet another embodiment, one of the two series of field effect  
2 transistors are isolated by shallow trench isolation, and different  
3 threshold voltages between the field effect transistors in different series  
4 are achieved by varying the active area widths of the field effect  
5 transistors in the series. At least one of the series preferably has active  
6 area widths less than one micron.

### 7 8 **BRIEF DESCRIPTION OF THE DRAWINGS**

9 Preferred embodiments of the invention are described below with  
10 reference to the following accompanying drawings.

11 Fig. 1 is a diagrammatic side sectional view of the semiconductor  
12 wafer fragment in process in accordance with one embodiment of the  
13 invention.

14 Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step  
15 which is subsequent to that which is shown in Fig. 1.

16 Fig. 3 is a plan view of the Fig. 1 wafer fragment at a processing  
17 step which is subsequent to that which is shown in Fig. 2.

18 Fig. 4 is a side view of the Fig. 3 wafer fragment.

19 Fig. 5 is a schematic diagram of circuitry formed in accordance  
20 with another embodiment of the invention.

21 Fig. 6 is a schematic diagram of circuitry formed in accordance  
22 with another embodiment of the invention.  
23

1           Fig. 7 is a schematic diagram of circuitry formed in accordance  
2 with another embodiment of the invention.

### 3 4           DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

5           This disclosure of the invention is submitted in furtherance of the  
6 constitutional purposes of the U.S. Patent Laws "to promote the progress  
7 of science and useful arts" (Article 1, Section 8).

8           Referring to Fig. 1, a semiconductor wafer fragment in process is  
9 shown generally at 10, and includes a semiconductive substrate 12. In  
10 the context of this document, the term "semiconductive substrate" is  
11 defined to mean any construction comprising semiconductive material,  
12 including, but not limited to, bulk semiconductive materials such as a  
13 semiconductive wafer (either alone or in assemblies comprising other  
14 materials thereon), and semiconductive material layers (either alone or  
15 in assemblies comprising other materials). The term "substrate" refers  
16 to any supporting structure, including, but not limited to, the  
17 semiconductive substrates described above.

18           Referring to Fig. 2, a plurality of active areas are formed over  
19 substrate 12, with an exemplary pair of active areas 14, 16 being shown.  
20 Active areas 14, 16 can constitute individual active sub-areas within a  
21 larger active area. In a preferred embodiment, active areas or sub-areas  
22 14, 16 are defined between a plurality of shallow trench isolation regions  
23 18 which are received within substrate 12. The spacing of shallow

trench isolation regions 18 defines a plurality of active area widths, with exemplary widths being shown at  $w_1$  and  $w_2$ . Preferably, at least two of the widths are different from one another. Of course, more than two of the widths could be different from one another.

In one embodiment, some of the active area widths are no greater than about one micron. One micron happens to be a break point that is technologically dependent. In other words, STI transistors show a threshold voltage reduction with reducing gate width when the gate width is about one micron or less. It will be understood that other sizes that correspond to a break point in threshold voltage versus gate width or control element size for transistors made using other technologies could be used instead of "one micron".

In one embodiment, one or both of widths  $w_1$  and  $w_2$  could be less than one micron. In a preferred embodiment, the different active area widths impart to transistors which are to be formed, different threshold voltages which, in a most preferred embodiment, are achieved without conducting or using a separate channel implant for the different transistors. Such results in a reduction in the number of processing steps which were previously required to form transistors having different threshold voltages.

In one embodiment, the different threshold voltages are each less than two volts. In another embodiment, the different threshold voltages are each less than one volt. In this example, the transistor having the

1 lower of the threshold voltages corresponds to the transistor which is  
2 formed relative to the active area having the lesser or smaller active  
3 area width.

4 With respect to provision of the channel implant(s) which defines  
5 the threshold voltages, one or more such implants can be conducted  
6 relative to the active areas. Preferably, each of the one or more  
7 channel implants are common to the transistors having the different  
8 active area widths which, in turn, provides transistors having different  
9 threshold voltages.

10 Fig. 3 is a plan view of the Fig. 1 wafer fragment at a processing  
11 step which is subsequent to that which is shown in Fig. 2, and Fig. 4  
12 is a side view of the Fig. 3 wafer fragment. A transistor gate line 20  
13 is formed over respective active areas 14, 16 to provide individual  
14 transistors, wherein the transistors corresponding to the active areas  
15 having the different active area widths have different threshold voltages  
16 as discussed above. Gate lines such as line 20 typically have a gate  
17 oxide layer, one or more conductive layers such as polysilicon and a  
18 silicide layer, one or more insulative caps, and insulative sidewall spacers  
19 (not shown), none of which are specifically designated. The illustrated  
20 gate line constitutes a common gate line which is formed over the  
21 illustrated active areas. It is, of course, possible to form separate gate  
22 lines over the active areas having the different widths.



Alternately considered, and in accordance with one embodiment of the present invention, two series of field effect transistors are formed over substrate 12. One of the series of field effect transistors (an exemplary transistor of which being formed over active area 14) is isolated from other adjacent devices by shallow trench isolation regions 18. The other series of field effect transistors (an exemplary transistor of which being formed over active area 16) has active area widths greater than one micron, with the first-mentioned series being formed to have active area widths less than one micron to achieve lower threshold voltages than the other of the series. Preferably, the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants. In a most preferred embodiment, the one or more common channel implants are the only implants which define the threshold voltages for the two series of field effect transistors.

Further and alternately considered, and in accordance with another embodiment of the present invention, the two series of field effect transistors just mentioned include at least one series which is isolated from adjacent devices by shallow trench isolation regions such as regions 18. Different threshold voltages are achieved between field effect transistors in the different series by varying the active area widths of the field effect transistors in the series, with at least one of the series having active area widths less than one micron, or less for future technologies.

1           Accordingly, field effect transistors can be fabricated having  
2 different threshold voltages without using a separate channel implant for  
3 the field effect transistors having the different threshold voltages. Such  
4 can result in a reduction in processing steps, which formerly included  
5 additional masking steps. One or more of the active areas can have  
6 widths less than one micron, with such widths being varied in order to  
7 change the threshold voltages of the transistors formed thereover.

8           In operation, various methods of the invention provide integrated  
9 circuitry having transistors with different threshold voltages without the  
10 added processing complexity. In a preferred embodiment, various  
11 methods of the invention can provide dynamic random access memory  
12 circuitry having a memory array area for supporting memory circuitry and  
13 a peripheral area for supporting peripheral circuitry. A plurality of  
14 shallow trench isolation regions are received within the peripheral area  
15 of the substrate and define a plurality of active areas having widths  
16 within the substrate, some of the widths being no greater than about  
17 one micron. Preferably, at least two of the widths are different. A  
18 conductive line is formed or disposed over the respective active areas to  
19 provide MOS gate electrodes for individual transistors. The transistors  
20 corresponding to the active areas having the different widths preferably  
21 have different threshold voltages. Exemplary dynamic random access  
22 memory circuitry is described in U.S. Pat. Nos. 5,702,990 and 5,686,747,  
23 which are incorporated by reference.

1 Referring to Fig. 5, a circuit 28 is provided and includes  
2 transistors 30, 32. Such transistors can be fabricated, in accordance with  
3 the methods described above, to have different threshold voltages. In  
4 this example, transistor 30 serves as a pass transistor and has a low  
5 threshold voltage  $V_{tl}$ , while transistor 32 serves as a switching transistor  
6 and has a high threshold voltage  $V_{th}$ .

7 Referring to Fig. 6, a circuit 34 is provided and includes  
8 transistors 36, 38 which can have different threshold voltages. Such  
9 circuit comprises a portion of precharge circuitry for dynamic random  
10 access memory circuitry. In the example of Fig. 6, the transistor 36 has  
11 a low threshold voltage  $V_{tl}$  and the transistor 38 has a high threshold  
12 voltage  $V_{th}$ .

13 Referring to Fig. 7, a circuit is shown generally at 40 and  
14 comprises transistors 42, 44 and 46 having threshold voltages  $V_{t1}$ ,  $V_{t2}$  and  
15  $V_{t3}$ , respectively. The transistors 42, 44 and 46 are fabricated to be  
16 formed in a parallel configuration with a common gate line 48  
17 interconnecting the transistors 42, 44 and 46 and coupling a signal  $C_{SAL}$   
18 to gates of the transistors. In this example, the transistors 42, 44, 46  
19 each have different active area widths which results in different threshold  
20 voltages.

21 Also shown in Fig. 7 is a sense amplifier circuit 50 including  
22 cross-coupled transistors 52 and 54. In one embodiment, the transistors  
23 52 and 54 are formed to have a low threshold voltage  $V_{tl}$ . When the

1 signal  $C_{SAL}$  goes to logic "1", the common node labeled RNL\*  
2 equilibrates the potentials on sources of the transistors 52 and 54 in  
3 preparation for reading stored data from memory cells in a memory  
4 array (not shown). In the example shown in Fig. 7, the circuit (40) acts  
5 as a pull-down circuit and equilibrates the node RNL\* to ground. Use  
6 of multiple transistors 42, 44 and 46 having different threshold voltages  
7 facilitates ("softens") sensing at the beginning of the sensing cycle and  
8 also more rapid sensing at the end of the cycle when differential signals  
9 have been developed by the transistors 52 and 54.

10 Advantages of the invention can include provision of a plurality of  
11 transistors having different threshold voltages, without the necessity of  
12 providing different dedicated processing steps to achieve such different  
13 threshold voltages. In various preferred embodiments, such results are  
14 attained through the use of shallow trench isolation and various so-called  
15 reverse narrow width characteristics. Additionally, current drive can be  
16 achieved using multiple narrow width devices in parallel ~~(Fig. 7)~~ <sup>of the same or different</sup>. The  $V_t$ 's  
17 invention can be useful for low threshold voltage applications such as  
18 precharge circuitry in DRAM circuitry, or as output drivers where low  
19 threshold voltages are important to obtain higher signal levels.

20 In compliance with the statute, the invention has been described  
21 in language more or less specific as to structural and methodical  
22 features. It is to be understood, however, that the invention is not  
23 limited to the specific features shown and described, since the means

1 herein disclosed comprise preferred forms of putting the invention into  
2 effect. The invention is, therefore, claimed in any of its forms or  
3 modifications within the proper scope of the appended claims  
4 appropriately interpreted in accordance with the doctrine of equivalents.  
5  
6  
7  
8  
9  
10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23